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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,995	11/12/2003	Hon-Chen Tsau	MSCP0017USA	2994

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EXAMINER
TRUJILLO, JAMES K

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,995	TSAU ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file:

2. Claims 1-17 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kawata, U.S. Patent 6,076,171.

5. Regarding claim 1, Kawata teaches a method for dynamically adjusting an operational frequency of a digital processing device comprising:

a. selecting a frequency operational mode (busy ratios (a)-(d) at times T0, T1, T2, T3 and T4, figures 3 and 4; states (1)-(4), figure 5);

b. setting a range of operational frequencies according to the frequency operational mode (frequencies within the busy ratios, figures 3 and 4); and

c. selecting an operational frequency within the frequency range for running the digital processing device (setting the system clock frequency to f4, col. 8, lines 51-58).

6. Regarding claim 2, Kawata taught the method according to claim 1, as described above. Kawata further teaches wherein the frequency operational mode is used for assigning a variation

tolerance of the operational frequency (permissible range for operating modes, figure 2; figure 5).

7. Regarding claim 4, Kawata taught the method according to claim 1, as described above. Kawata further teaches the method capable of being used for adjusting the operational frequency by changing a core clock, a memory clock or both of them (system clock or memory, col. 10, lines 33-47 and col. 11, lines 17-45).

8. Regarding claim 5, Kawata taught the method according to claim 1, as described above. Kawata further teaches the being performed in a central processing unit (CPU 20, col. 10, lines 33-47).

9. Regarding claim 6, Kawata teaches a method for dynamically adjusting an operational frequency of a digital processing device comprising:

a. (a) setting a frequency range (busy ratios (a)-(d) at times T0, T1, T2, T3 and T4, figures 3 and 4; and frequencies for states (1)-(4), figure 5); and

b. (b) selecting an operational frequency in the frequency range for running the digital processing device (f4, figures 3, 4 and col. 8, lines 48-58).

10. Regarding claim 7, Kawata taught the method according to claim 6, as described above. Kawata further teaches wherein step (a) further comprises:

a. (a1) selecting a frequency operational mode (wherein the modes are the states, figure 5); and

b. (a2) setting a range of operational frequencies according to the frequency operational mode (wherein the ranges are the permissible ranges for the modes, figures 2-5).

11. Regarding claim 8, Kawata taught the method according to claim 7, as described above. Kawata further teaches wherein the frequency operational mode is used for assigning a variation tolerance of the operational frequency (permissible range for operating modes, figure 2; figure 5).

12. Regarding claims 10 and 11, they are rejected for the same reasons as set forth in the rejection of claims 4 and 5, respectively, described above.

13. Regarding claim 12, Kawata taught the method according to claim 6, as described above. Kawata appears to teach further comprising determining being enabled by a user (frequency and duty factor may be set, col. 4, lines 51-67;a user is able to select clock states, col. 20, lines 5-15).

14. Regarding claim 13, Kawata teaches a system for dynamically adjusting an operational frequency of a digital processing device, comprising:

a. an interface unit for receiving an external command to select a frequency operational mode (an interface unit is inherent in order to receive the selection by the user, col. 20, lines 6-14);

b. a setting unit (sweep circuit 52, figure 7), coupled to the interface unit, for setting a frequency range according to the frequency operational mode (figure 7 and col. 10, line 50 through col. 11, line 11); and

c. a processing unit, coupled to the setting unit, for selecting an operational frequency in the frequency range (CPU 20, figure 6 and col. 10, lines 33-47).

15. Regarding claim 14, Kawata taught the system according to claim 13, as described above. Kawata further teaches wherein the frequency operational mode is used for assigning a variation

tolerance of the operational frequency (permissible range for operating modes, figure 2; figure 5).

16. Regarding claim 15, Kawata taught the system according to claim 13, as described above. Kawata further teaches wherein the operational frequency is capable of being adjusted by changing a core clock, a memory clock or both of them (system clock or memory, col. 10, lines 33-47 and col. 11, lines 17-45).

17. Regarding claim 16, Kawata taught the system according to claim 13, as described above. Kawata further teaches wherein capable of determining being enabled by a user (frequency and duty factor may be set, col. 4, lines 51-67;a user is able to select clock states, col. 20, lines 5-15).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 3 and 9 are rejected under 35 U.S.C. 102(b) as anticipated by Kawata or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kawata or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kawata in view of Applicant's Admitted Prior Art (AAPA).

20. Regarding claim 3, Kawata taught the method according to claim 1, as described above. Kawata further appears to teach wherein the method is being performed in a video graphics adapter (system clock for a display is being adjusted, col. 10, lines 33-47 and col. 11, lines 17-45). Even if Kawata does not teach wherein the method is being perform in a video graphics

adapter, Applicant(s) numerous components (VGA, CPU, Memory, Core clock) of where the method is applied (in claims 3-5) is construed to be an admission that the criticality does not reside in the where the method is performed and hence obvious variations of one another. Further, even if Kawata does not teach wherein the method is being performed in a video graphics adapter, AAPA teaches a system that uses a GPU in VGA for graphics processing (paragraph [0006]). It would have been obvious to one of ordinary skill in the art, having the teachings of Kawata and AAPA before them at the time the invention was made, to modify the teachings of Kawata by performing his method to a GPU in VGA. One of ordinary skill in the art would have been motivated to make the modification in order to achieve the advantage of reducing power consumption without causing discomfort to the user (col. 2, lines 20-31) in a VGA.

21. Regarding claim 9, Kawata or in the alternative of Kawata in view of AAPA taught the claimed method therefore they teach the claimed system.

22. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawata. Kawata taught the system according to claim 13, as described above. Kawata does not explicitly disclose wherein the setting unit built within the processing unit. Kawata has both a setting unit and a processing unit, however the setting unit is not built within the processing unit.

The examiner takes Official Notice of integrating functional units together. As is well known in the electrical and computer arts, integrating functional units provide the advantages of reducing cost, reducing space, reducing power consumption, increasing processing speed, and increasing reliability.

It would have been obvious to one of ordinary skill in the art having the teachings of Kawata and the knowledge of integrating functional units to modify the setting unit of Kawata by building it within the processing by integrating it within the processing unit.

One of ordinary skill in the art would have been motivated to make this modification in order to achieve the advantages of reducing cost, reducing space, reducing power consumption, increasing processing speed, and increasing reliability.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 5,958,058 to Barrus teaches a system that allows a user to select the CPU operating frequency.

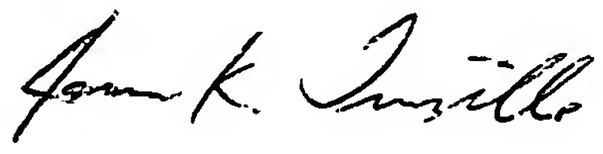
U.S. Pat. No. 6,037,814 to Hirakawa teaches a system having an oscillator that operates near the center of an operating range.

U.S. Pat. No. 6,580,432 to Leung et al., teaches a system that uses a spread spectrum clock.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (8:00 am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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